HARDWARE

REFERENCE DESIGN

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UM681 Series

Multi-System Dual-Frequency High-Precision RTK Integrated Positioning Module

Revision History

Version	Revision History	Date
R1.0	First release.	May 2025

Document Status

Releases	Status Descriptions	Current Status
Primary	This is a pre-release version with target specifications that are subject to revision.	
Alpha release	This is an alpha release version, which has been preliminarily tested and verified. The content may undergo minor modifications based on user feedback and further testing.	
Production release	The document contains the complete and final specifications.	√

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Foreword

This document provides the hardware reference design of Unicore UM681 series modules.

UM681 series modules consist of the following models:

Product	Main model	Sub-Model
UM681 series	UM681A (automotive)	UM681A-12
	UM681 (industrial)	UM681-12

Target Readers

This document applies to technicians who are familiar with GNSS receivers.

Contents

1 Block Diagram

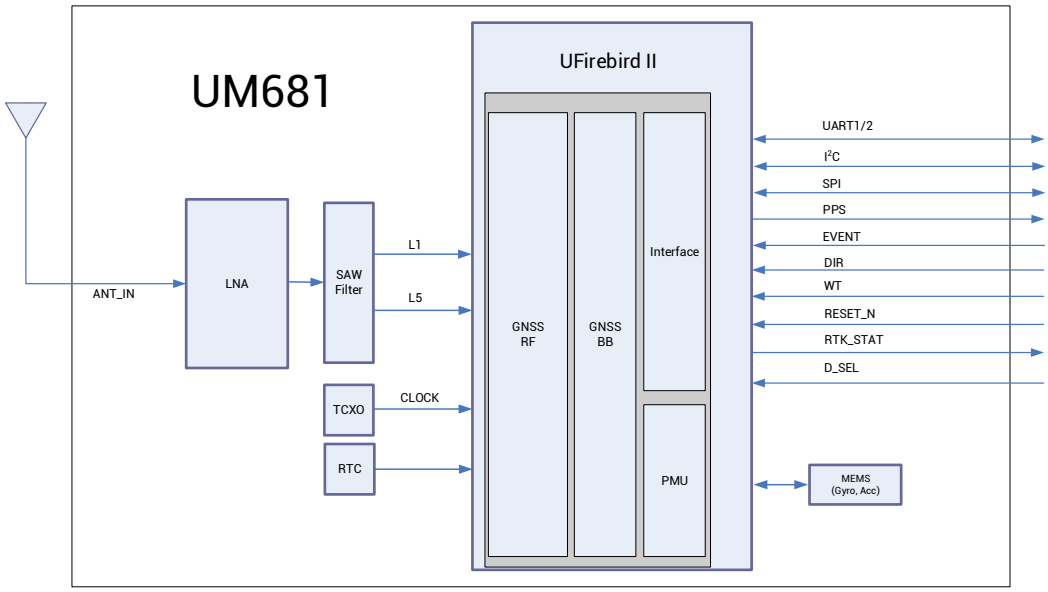


Figure 1-1 UM681 Block Diagram[1]

[1] SPIS and I²C/UART1 share the same pins.

2 UM681 Peripheral Design

- Connect the ANT_IN signal to the antenna, and note the 50 Ω impedance matching.
- Connect all the GND pins to the ground.
- Leave the IO pins open if not used.
- Recommended to add TVS anti-surge protection at the power input of the module. Add ESD protection at all the used pins.

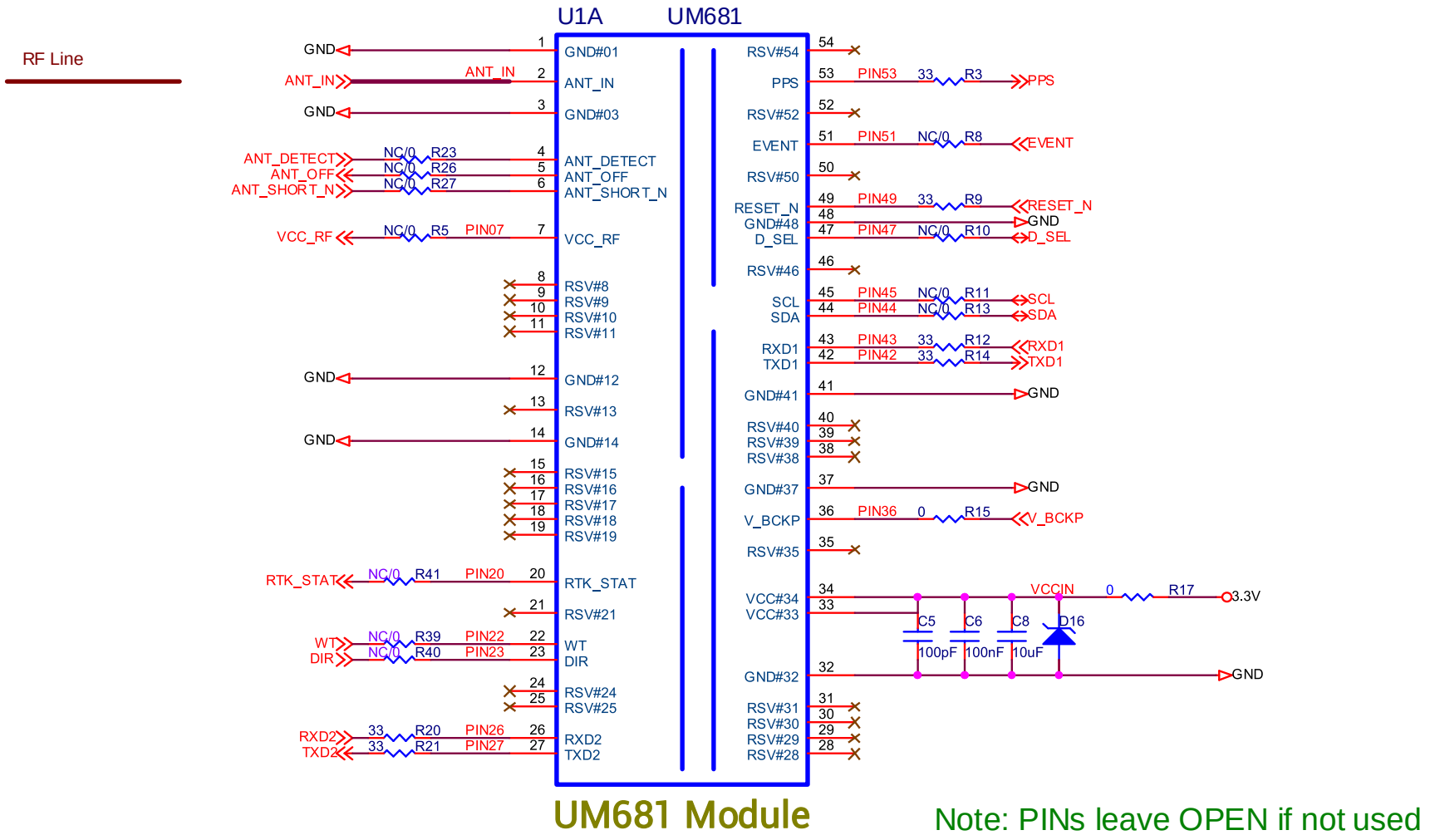


Figure 2-1 UM681 Peripheral Design[1]

The GND pads at the bottom of the module should be grounded to ensure heat dissipation.

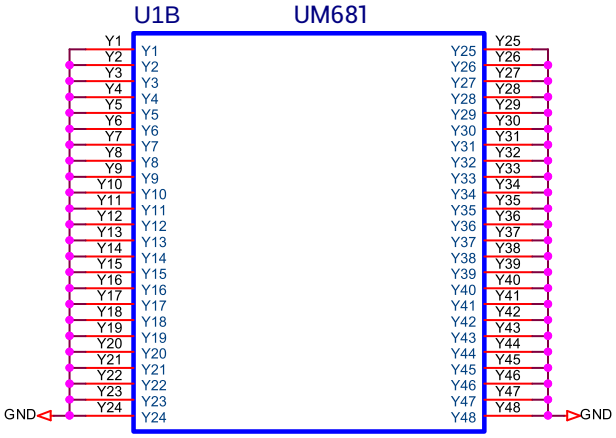


Figure 2-2 UM681 GND Pads

2.1 Main Power VCC

The working voltage range of VCC is 2.7 V to 3.6 V.

Note:

- The VCC initial level when power-on should be less than 0.4 V.
- The VCC ramp when power-on should be monotonic, without plateaus.
- The voltages of undershoot and ringing should be within 5% VCC.
- VCC power-on waveform: The time interval from 10% rising to 90% must be within 100 μs to 10 ms.
- Power-on time interval: The time interval between the power-off (VCC < 0.4 V) to the next power-on must be larger than 500 ms.

2.2 Backup Power V_BCKP

When using the hot start function, please provide backup power for the module. The input range of V_BCKP is 2.0 V to 3.6 V.

Note:

- The V_BCKP initial level when power-on should be less than 0.4 V.
- The V_BCKP ramp when power-on should be monotonic, without plateaus.
- The voltages of undershoot and ringing should be within 5% V_BCKP.
- V_BCKP power-on waveform: The time interval from 10% rising to 90% must be within 100 μs to 10 ms.
- Power-on time interval: The time interval between the power-off (V_BCKP < 0.4 V)

to the next power-on must be larger than 500 ms.

- When the hot start function is not used, connect V_BCKP to VCC or a backup power source. Do not connect it to ground or leave it floating.

2.3 Active Antenna Feed Circuit

The antenna feed circuit consists of the anti-surge design, filter inductors, and ESD protection. The ESD protection diode should support high-frequency signals (above 2000 MHz).

☞ It is not recommended to use VCC_RF to feed the antenna. VCC_RF has not been optimized for the anti-lightning strike and anti-surge due to the compact size of the module.

☞ If the antenna feed supply ANT_BIAS and the module's main supply VCC use the same power rail, the ESD, surge and overvoltage generated at the antenna will be directly applied to VCC, which may cause damage to the module. Therefore, it is recommended to design an independent power rail for the ANT_BIAS to reduce the possibility of module damage.

Connect the ANT_IN signal to the antenna, and note the 50 Ω impedance matching.

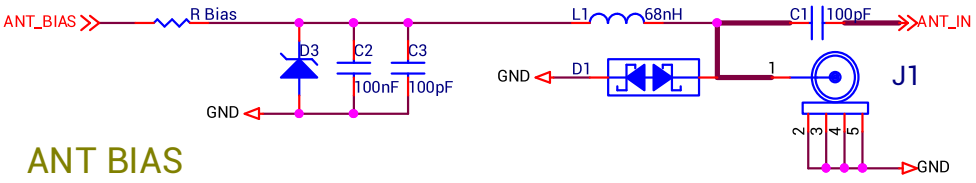
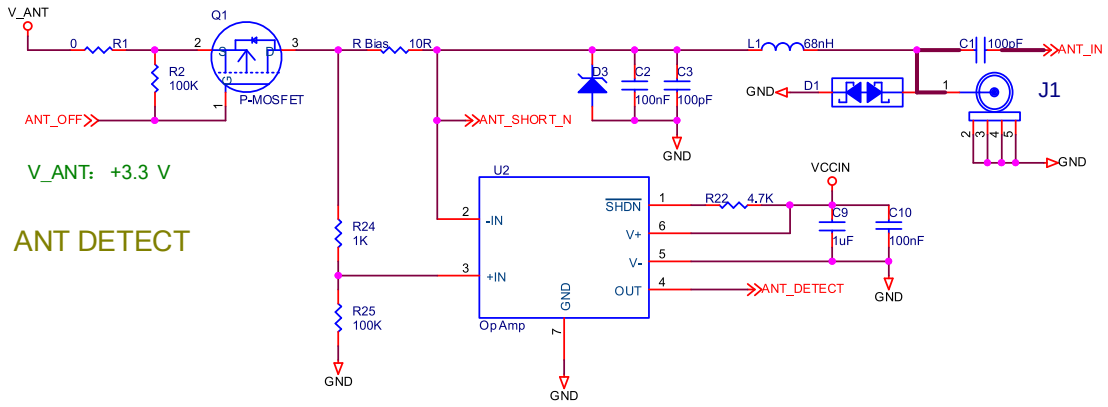


Figure 2-3 Antenna Feed Circuit

2.4 Antenna Detection Circuit

UM681 supports antenna status detection and the circuit is shown as follows:



Note: I/O Buffer is required when V_ANT&VCCIN voltage not matched

Figure 2-4 Antenna Detection Circuit

Status	ANT_DETECT	ANT_SHORT_N	ANT_OFF
Open	0	1	0
Short	1	0	1
OK	1	1	0

2.5 Reset Circuit

UM681 supports system reset. The pin RESET_N is active low and the active time should be no less than 5 ms.

3 Odometer Interfaces

Odometer data can be input to the UM681 module via hardware interface or software interface.

☞ The two ways cannot be used at the same time.

3.1 Hardware Interface

The pin 22 (WT) of the UM681 module is used to receive the speed pulse signal (WHEELTICK) from the odometer, and the pin 23 (DIR) is used to receive the direction signal (FWD) from the odometer.

The odometer signal of vehicles is generally 12 V and the signal quality is poor. Therefore, signal filtering, optocoupler isolation and level conversion are required before transferring the odometer signal to the UM681 module for use.

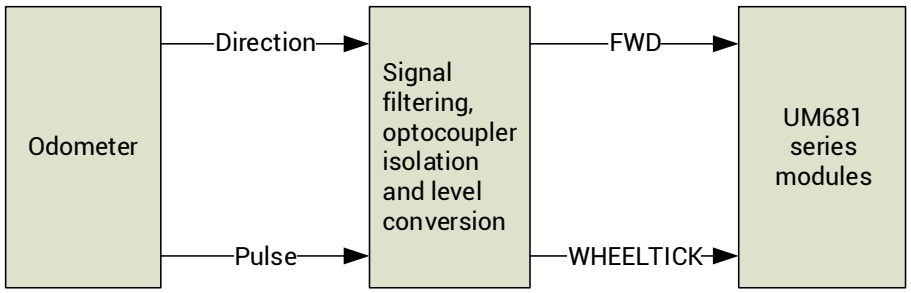


Figure 3-1 Odometer Connection

3.1.1 Odometer Reference Circuit and Waveform Diagram

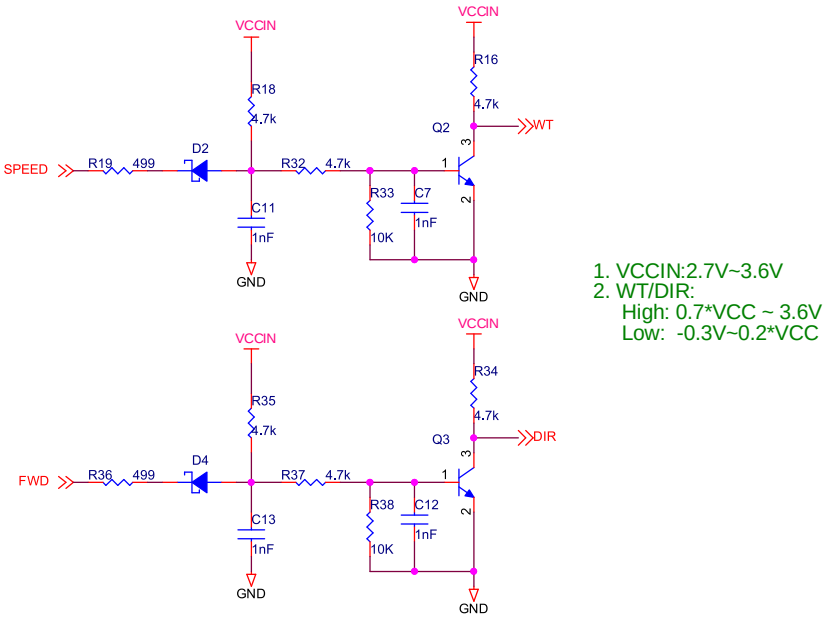


Figure 3-2 Reference Circuit for Odometer

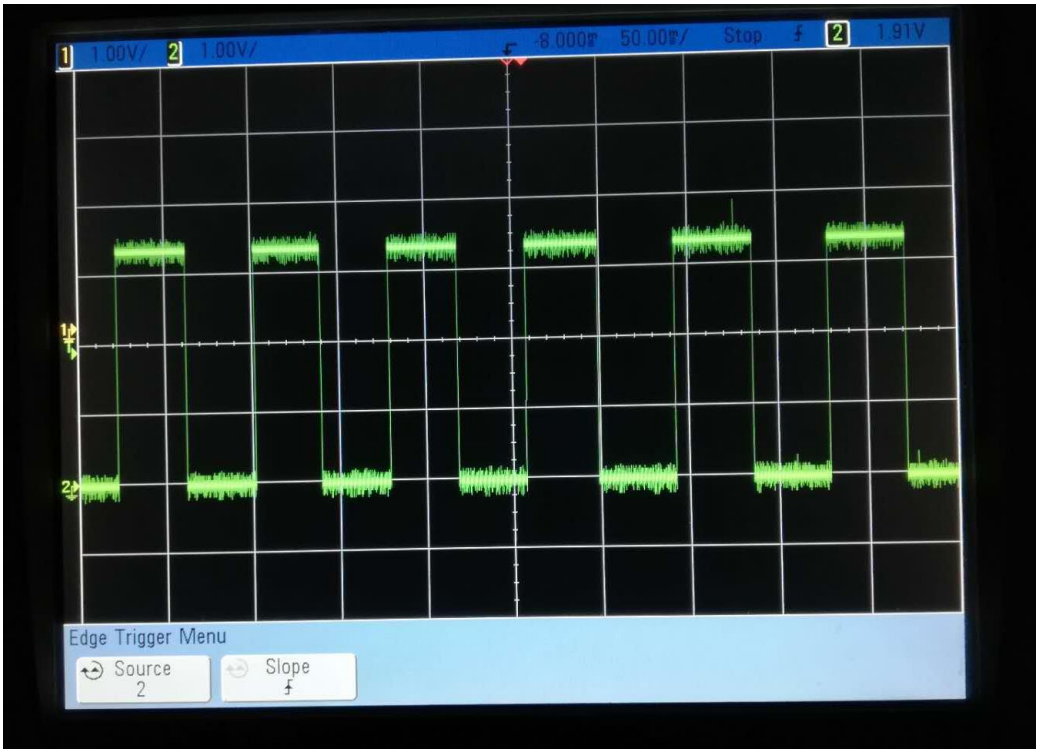


Figure 3-3 Odometer Waveform Diagram

3.1.2 Odometer Speed and Direction Signals

3.1.2.1 Voltage Requirements

The voltage requirements for VCC, V_BCKP, WT and DIR are shown in **Table 3-1**.

Table 3-1 Voltage Requirements

Item	Symbol	Min.	Typ.	Max.	Unit
Main Supply	VCC	2.7	3.3	3.6	V
Backup Supply	V_BCKP	2.0		3.6	V
Ripple Voltage	V_{p-p}			50	mV
WT/DIR Low Level Input Voltage	V_{IL}	-0.3		0.2*VCC	V
WT/DIR High Level Input Voltage	V_{IH}	0.7*VCC		3.6	V

3.1.2.2 Speed Signal (WHEELTICK)

1. The speed signal input to the module is required to be a square wave signal, and the frequency shall not exceed 5 KHz.
2. The pulse width of a square wave signal is required to be between 1 cm and 40 cm. For example, if the pulse width is 20 cm, the output frequency is

   $$f = [(1000/20) * V/36] Hz$$

   where V is the velocity of the vehicle and its unit is km/h.
3. The chip detects the number of rising edges of the square wave signal, and the time of high level and low level shall be no less than 100 μs.
4. If the vehicle is still (for example, parking), the level of the WT pin must remain constant.

3.1.2.3 Direction Signal (FWD)

The module defaults to forward at high level and reverse at low level.

It can be configured through the commands as shown below. For more information, please refer to the protocol manual.

$CFGODOFWD,1 *forward at high level and reverse at low level (by default)*
$CFGODOFWD,0 *forward at low level and reverse at high level*

3.2 Software Interface

Speed and direction information can be input to the UM681 module via UART1 or UART2, which can be configured by the following command.

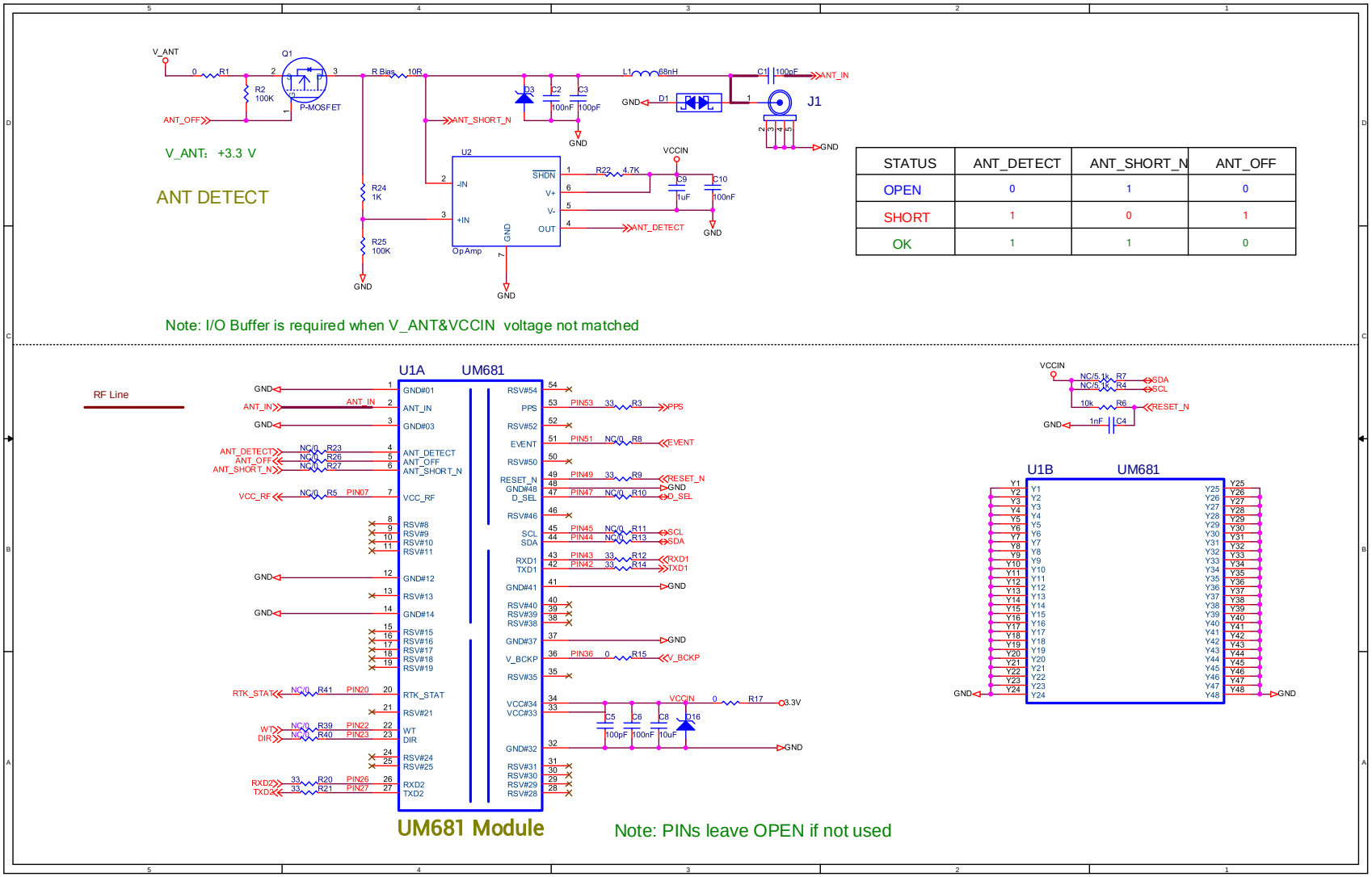
Syntax: $ODODATA,time,speed,forward,RSV,RSV,RSV

Example: $ODODATA,091649.00,10000,1,,,

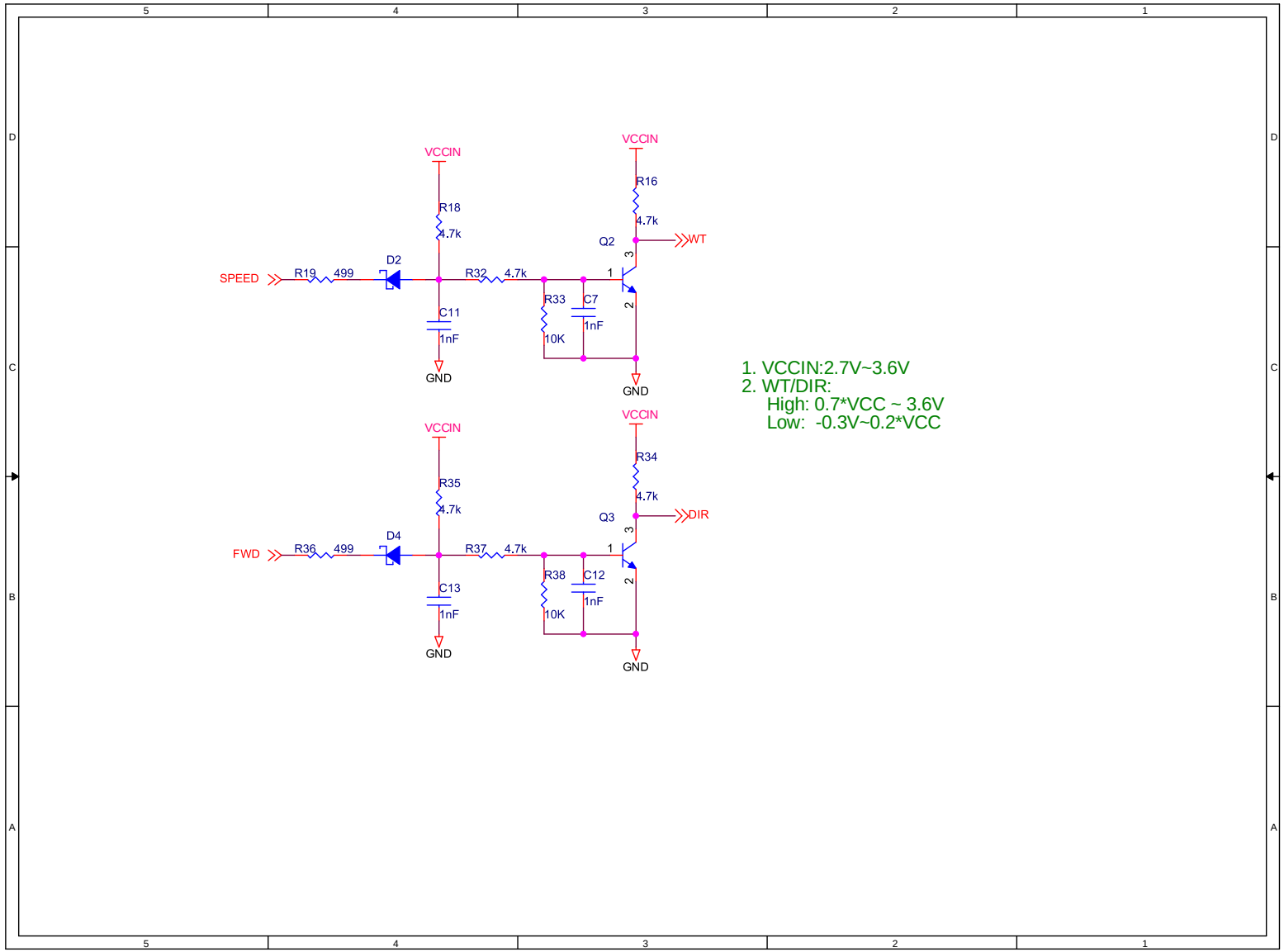
Table 3-4 Parameter Description of ODODATA

Parameter	Format	Description
time	STR	UTC time; in the format of hhmmss.ss hh - Hour mm - Minute ss.ss - Second
speed	UINT	Driving speed; unit: 1e-3 m/s
forward	UINT	Driving direction: 0 - Forward 1 - Reverse
RSV		Reserved
RSV		Reserved
RSV		Reserved

4 Appendix: Schematics of Reference Design



STATUS	ANT_DETECT	ANT_SHORT_N	ANT_OFF
OPEN	0	1	0
SHORT	1	0	1
OK	1	1	0


VCCIN
R18
4.7k
SPEED
R19
499
D2
R32
4.7k
C11
1nF
GND
VCCIN
R16
4.7k
Q2
WT
R33
10K
C7
1nF
GND
VCCIN
R35
4.7k
FWD
R36
499
D4
R37
4.7k
C13
1nF
GND
VCCIN
R34
4.7k
Q3
DIR
R38
10K
C12
1nF
GND
1. VCCIN:2.7V~3.6V
2. WT/DIR:
High: 0.7*VCC ~ 3.6V
Low: -0.3V~0.2*VCC

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